This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A semiconductor integrated circuit having a high voltage generator for generating a boosted internal power supply potential, the high voltage generator comprising:

a plurality of first capacitors that are charged during a first period;

a plurality of second capacitors provided alternately with the first capacitors, the second capacitors being charged during a second period ~~that partially overlaps with the first period~~;

a first potential converter for supplying a boosted clock to each first capacitor;

a second potential converter for supplying a boosted clock to each second capacitor;

a first transfer device for transferring charges stored in each first capacitor to the succeeding second capacitor during a third period that is delayed from the second period by a predetermined time; and

a second transfer device for transferring charges stored in each second capacitor to the succeeding first capacitor during a fourth period that is delayed from the first period by ~~the~~ a predetermined time.

Claim 2 (currently amended): The semiconductor integrated circuit according to claim 1, wherein the first transfer device includes a first NMOS transistor, a source thereof being connected to each first capacitor, a drain thereof being connected to the succeeding second capacitor, the high voltage generator further including:

a third capacitor connected to a gate of the first NMOS transistor; and

a second NMOS transistor, a source thereof being connected to the source of the first NMOS transistor, a drain thereof being connected to the gate of the first NMOS transistor and a gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on during a period in which the first and the second periods overlap each other to charge the third capacitor, and charges stored in the third capacitor are supplied to the gate of the first NMOS transistor as the first transfer device

during the third period, charges stored in each first capacitor being transferred to the succeeding second capacitor via the first transfer device thus turned on.

Claim 3 (currently amended): The semiconductor integrated circuit according to claim 1, wherein the second transfer device includes a first NMOS transistor, a source thereof being connected to each second capacitor, a drain thereof being connected to the succeeding first capacitor, the high voltage generator further including:

a third capacitor connected to a gate of the first NMOS transistor; and

a second NMOS transistor, a source thereof being connected to the source of the first NMOS transistor, a drain thereof being connected to the gate of the first NMOS transistor and a gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on during a period in which the first and the second periods overlap each other to charge the third capacitor, and charges stored in the third capacitor ~~is~~ are supplied to the gate of the first NMOS transistor as the second transfer device during the fourth period, charges stored in each second capacitor being transferred to the succeeding first capacitor via the second transfer device thus turned on.

Claim 4 (currently amended): The semiconductor integrated circuit according to claim 1, wherein the third period terminates by ~~the~~ a predetermined time before the succeeding second period starts.

Claim 5 (currently amended): The semiconductor integrated circuit according to claim 1, wherein the fourth period terminates by ~~the~~ a predetermined time before the succeeding first period starts.

Claim 6 (new): The semiconductor integrated circuit according to claim 1, wherein the first potential converter includes a third capacitor that is charged during a period in which the boosted clock to be supplied to each first capacitor is at a first level, a first terminal of the third capacitor being electrically coupled to each first capacitor and a second terminal of the third capacitor

being supplied a voltage higher than zero volts during a period in which the boosted clock to be supplied to each first capacitor is at a second level higher than the first level.

Claim 7 (new): The semiconductor integrated circuit according to claim 6, wherein the first transfer device includes a first NMOS transistor, the source thereof being connected to each first capacitor, the drain thereof being connected to the succeeding second capacitor, the high voltage generator further including:

a fourth capacitor connected to the gate of the first NMOS transistor; and

a second NMOS transistor, the source thereof being connected to the source of the first NMOS transistor, the drain thereof being connected to the gate of the first NMOS transistor and the gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on during a period in which the first and the second periods overlap each other to charge the fourth capacitor, and charges stored in the fourth capacitor are supplied to the gate of the first NMOS transistor as the first transfer device during the third period, charges stored in each first capacitor being transferred to the succeeding second capacitor via the first transfer device thus turned on.

Claim 8 (new): The semiconductor integrated circuit according to claim 6, wherein the second transfer device includes a first NMOS transistor, the source thereof being connected to each second capacitor, the drain thereof being connected to the succeeding first capacitor, the high voltage generator further including:

a fourth capacitor connected to the gate of the first NMOS transistor; and

a second NMOS transistor, the source thereof being connected to the source of the first NMOS transistor, the drain thereof being connected to the gate of the first NMOS transistor and the gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on during a period in which the first and the second periods overlap each other to charge the fourth capacitor, and charges stored in the fourth capacitor are supplied to the gate of the first NMOS transistor as the second transfer device during the fourth period, charges stored in each second capacitor being transferred to the succeeding first capacitor via the second transfer device thus turned on.

Claim 9 (new): The semiconductor integrated circuit according to claim 6, wherein the third period terminates by a predetermined time before the succeeding second period starts.

Claim 10 (new): The semiconductor integrated circuit according to claim 6, wherein the fourth period terminates by a predetermined time before the succeeding first period starts.

Claim 11 (new): The semiconductor integrated circuit according to claim 1, wherein the second potential converter includes a third capacitor that is charged during a period in which the boosted clock to be supplied to each second capacitor is at a first level, a first terminal of the third capacitor being electrically coupled to each second capacitor and a second terminal of the third capacitor being supplied a voltage higher than zero volts during a period in which the boosted clock to be supplied to each second capacitor is at a second level higher than the first level.

Claim 12 (new): The semiconductor integrated circuit according to claim 11, wherein the first transfer device includes a first NMOS transistor, the source thereof being connected to each first capacitor, the drain thereof being connected to the succeeding second capacitor, the high voltage generator further including:

a fourth capacitor connected to the gate of the first NMOS transistor; and

a second NMOS transistor, the source thereof being connected to the source of the first NMOS transistor, the drain thereof being connected to the gate of the first NMOS transistor and the gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on during a period in which the first and the second periods overlap each other to charge the fourth capacitor, and charges stored in the fourth capacitor are supplied to the gate of the first NMOS transistor as the first transfer device during the third period, charges stored in each first capacitor being transferred to the succeeding second capacitor via the first transfer device thus turned on.

Claim 13 (new): The semiconductor integrated circuit according to claim 11, wherein the second transfer device includes a first NMOS transistor, the source thereof being connected to each second capacitor, the drain thereof being connected to the succeeding first capacitor, the high voltage generator further including:

a fourth capacitor connected to the gate of the first NMOS transistor; and

a second NMOS transistor, the source thereof being connected to the source of the first NMOS transistor, the drain thereof being connected to the gate of the first NMOS transistor and the gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on a period in which the first and the second periods overlap each other to charge the fourth capacitor, and charges stored in the fourth capacitor are supplied to the gate of the first NMOS transistor as the second transfer device during the fourth period, charges stored in each second capacitor being transferred to the succeeding first capacitor via the second transfer device thus turned on.

Claim 14 (new): The semiconductor integrated circuit according to claim 11, wherein the third period terminates by a predetermined time before the succeeding second period starts.

Claim 15 (new): The semiconductor integrated circuit according to claim 11, wherein the fourth period terminates by a predetermined time before the succeeding first period starts.

Claim 16 (new): The semiconductor integrated circuit according to claim 1, wherein the first potential converter includes:

a third capacitor, a first terminal thereof being connected to a high-level side power terminal via a first switching device, a second terminal thereof being connected to a low-level side power terminal via a second switching device that is turned on simultaneously with the first switching device;

a third switching device that is turned on in opposite timing for the first and the second switching devices to supply a driving potential to the second terminal of the third capacitor;

a fourth switching device that is turned on simultaneously with the third switching device to connect the first terminal of the third capacitor to an output terminal; and

a fifth switching device that is turned on simultaneously with the first switching device to reset a potential at the output terminal,

wherein the third capacitor is charged while the first and the second switching devices are on and the charged third capacitor is coupled to the first capacitor in series while the third and the fourth switching devices are on.

Claim 17 (new): The semiconductor integrated circuit according to claim 16, wherein the first transfer device includes a first NMOS transistor, the source thereof being connected to each first capacitor, the drain thereof being connected to the succeeding second capacitor, the high voltage generator further including:

a fourth capacitor connected to the gate of the first NMOS transistor; and

a second NMOS transistor, the source thereof being connected to the source of the first NMOS transistor, the drain thereof being connected to the gate of the first NMOS transistor and the gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on during a period in which the first and the second periods overlap each other to charge the fourth capacitor, and charges stored in the fourth capacitor are supplied to the gate of the first NMOS transistor as the first transfer device during the third period, charges stored in each first capacitor being transferred to the succeeding second capacitor via the first transfer device thus turned on.

Claim 18 (new): The semiconductor integrated circuit according to claim 16, wherein the second transfer device includes a first NMOS transistor, the source thereof being connected to each second capacitor, the drain thereof being connected to the succeeding first capacitor, the high voltage generator further including:

a fourth capacitor connected to the gate of the first NMOS transistor; and

a second NMOS transistor, the source thereof being connected to the source of the first NMOS transistor, the drain thereof being connected to the gate of the first NMOS transistor and the gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on a period in which the first and the second periods overlap each other to charge the fourth capacitor, and charges stored in the fourth capacitor are supplied to the gate of the first NMOS transistor as the second transfer device during the fourth period, charges stored in each second capacitor being transferred to the succeeding first capacitor via the second transfer device thus turned on.

Claim 19 (new): The semiconductor integrated circuit according to claim 16, wherein the third period terminates by a predetermined time before the succeeding second period starts.

Claim 20 (new): The semiconductor integrated circuit according to claim 16, wherein the fourth period terminates by a predetermined time before the succeeding first period starts.

Claim 21 (new): The semiconductor integrated circuit according to claim 1, wherein the second potential converters includes:

a third capacitor, a first terminal thereof being connected to a high-level side power terminal via a first switching device, a second terminal thereof being connected to a low-level side power terminal via a second switching device that is turned on simultaneously with the first switching device;

a third switching device that is turned on in opposite timing for the first and the second switching devices to supply a driving potential to the second terminal of the third capacitor;

a fourth switching device that is turned on simultaneously with the third switching device to connect the first terminal of the third capacitor to an output terminal; and

a fifth switch device that is turned on simultaneously with the first switching device to reset a potential at the output terminal,

wherein the third capacitor is charged while the first and the second switching devices are on and the charged third capacitor is coupled to the first capacitor in series while the third and the fourth switching devices are on.

Claim 22 (new): The semiconductor integrated circuit according to claim 21, wherein the first transfer device includes a first NMOS transistor, the source thereof being connected to each first

capacitor, the drain thereof being connected to the succeeding second capacitor, the high voltage generator further including:

a fourth capacitor connected to the gate of the first NMOS transistor; and

a second NMOS transistor, the source thereof being connected to the source of the first NMOS transistor, the drain thereof being connected to the gate of the first NMOS transistor and the gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on during a period in which the first and the second periods overlap each other to charge the fourth capacitor, and charges stored in the fourth capacitor are supplied to the gate of the first NMOS transistor as the first transfer device during the third period, charges stored in each first capacitor being transferred to the succeeding second capacitor via the first transfer device thus turned on.

Claim 23 (new): The semiconductor integrated circuit according to claim 21, wherein the second transfer device includes a first NMOS transistor, the source thereof being connected to each second capacitor, the drain thereof being connected to the succeeding first capacitor, the high voltage generator further including:

a fourth capacitor connected to the gate of the first NMOS transistor; and

a second NMOS transistor, the source thereof being connected to the source of the first NMOS transistor, the drain thereof being connected to the gate of the first NMOS transistor and the gate thereof being connected to the drain of the first NMOS transistor,

wherein the second NMOS transistor is turned on a period in which the first and the second periods overlap each other to charge the fourth capacitor, and charges stored in the fourth capacitor are supplied to the gate of the first NMOS transistor as the second transfer device during the fourth period, charges stored in each second capacitor being transferred to the succeeding first capacitor via the second transfer device thus turned on.

Claim 24 (new): The semiconductor integrated circuit according to claim 21, wherein the third period terminates by a predetermined time before the succeeding second period starts.

Claim 25 (new): The semiconductor integrated circuit according to claim 21, wherein the fourth period terminates by a predetermined time before the succeeding first period starts.